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POWER AND DELAY OPTIMIZATION IN FULL ADDER CIRCUIT USING DIFFERENT TECHNIQUES

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ABSTRACT

The Full Adder circuit is an important component in application such as Digital Signal Processing (DSP) architecture, microprocessor, microcontroller and data processing units. This paper discusses the evolution of full adder circuits in terms of lesser power consumption and higher speed. Starting with the most conventional 28 transistors full adder and then gradually studied different types of full adders. This paper has also included some of the most popular full adder cells like Transmission gate full adder, pass transistor full adder, Static Energy Recovery Full Adder (SERF), Adder9B, GDI based full adder and Self resetting logic(SRL) with GDI full adder. The simulations have been carried out by Tanner EDA tools on 250nm technology.

KEYWORDS: CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL), Gate Diffusion Input (GDI), Static Energy Recovery Full Adder (SERF)), Adder 9B, GDI based Full Adder, low power, Full Adder, CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), Self Resetting Logic(SRL)

INTRODUCTION

Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power consumption is one of the most critical design parameters. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power consumption. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. The reduction of the power consumption and the improvement of the speed require optimizations at all levels of the design procedure. Since, most digital circuitry is composed of simple and/or complex gates; the best way to implement adders in order to achieve low power consumption and high speed. Several circuit design techniques are compared in order to find their efficiency in terms of speed and power consumption.

At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Computations need to be performed using low- power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices. There is no ideal full adder cell that can be used in all types of applications. Hence novel architectures such as Static Energy Recovery Full Adder (SERF), Transmission Gate (TG), Adder 9B and GDI based full adder are proposed to meet the requirements.

The one-bit full adder has a three-input two-output building block. The inputs are the two bits to be summed A, B and the carry bit Cin, which derives from the calculations of the last stages digit. The outputs are the result of the sum operation S and the resulting value of the carry bit Cout. More expressly the sum and carry output are given by,

Sum = *A* xor *B* xor *C* … (1)

Cout = (*A* and *B*) or (*B* and *C*) or (*A* and *C*) … (2)

From (2) it is evident that if A=B the carry output is equal to their value.

DIFFERENT TYPES OF FULL ADDER CIRCUITS

In this section the different types of full adder circuits are discussed.

Conventional 28T CMOS Full Adder

Table 1: Truth Table of Full Adder

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

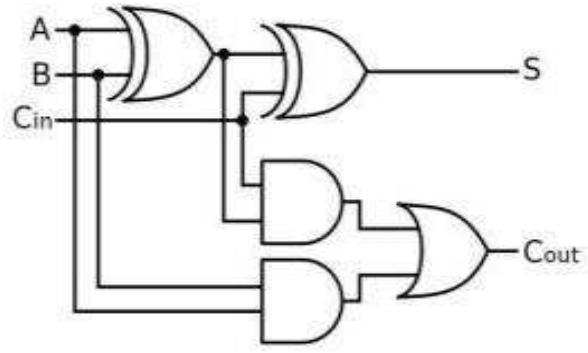

Figure 1: Block Diagram of Full Adder

The conventional CMOS adder cell using 28 transistors based on standard CMOS topology is shown in figure 2 Due to high number of transistors; its power consumption is high. Large PMOS transistor in pull up network results in high input capacitances, which cause high power consumption. One of the most significant advantages of this full adder was high noise margins and thus reliable operation at low voltages and high noise margin.

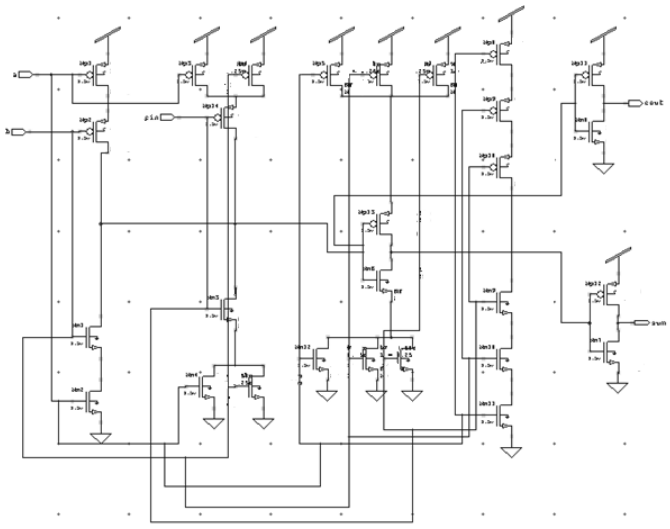

Figure 2: 28T Conventional CMOS Full Adder Circuit

Transmission Gate Full Adder

Transmission gate produces buffered outputs of proper polarity for both sum and carry. In this circuit two inverters are followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. It has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used generate sum; B and Cin are multiplexed which can generate cout. The signal cin controlled either by (*a* and b) or (a xor b).Similarly the cout can be calculated by multiplexing *a* and cin which is controlled by (a) and Cin are multiplexed which can controlled either by (a and b). The power dissipation in this circuit is more than the 28T or (a xor b).

Similarly the cout can be calculated by multiplexing *a* and cin controlled by (a and b). The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster.

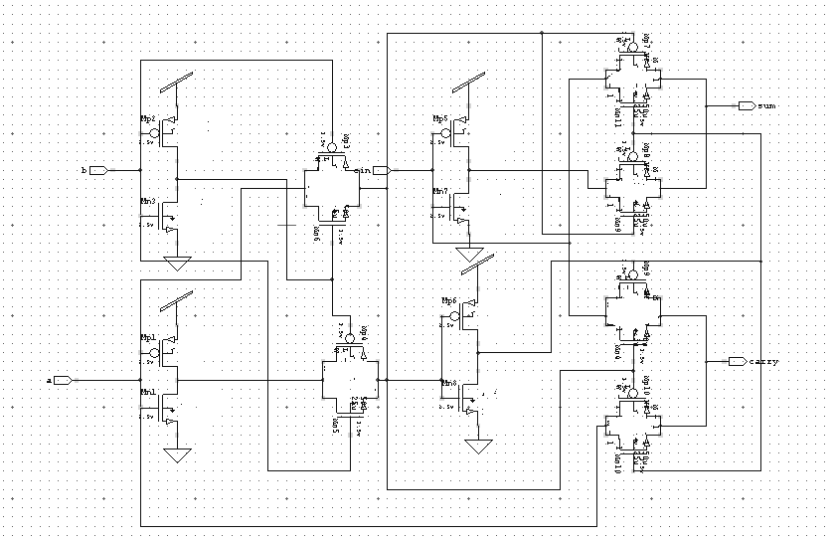

Figure 3: Transmission Gate Full Adder Circuit

Pass Transistor Full Adder

The 14 transistors used to realize the adder function. This design is area efficient. The 14 transistors adder circuits

are similar to transmission gate adder cell and implements the complementary pass logic to drive the load. Schematic diagram of adder using pass transistor full adder is given below,

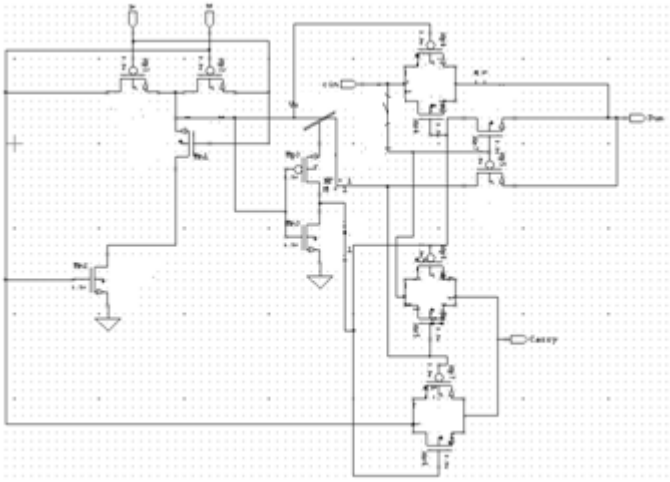

Figure 4: 14T Full Adder Circuit

Static Energy Recovery Full Adder

In the 10T adder cell, the implementation of XOR and XNOR of A and B are done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delay at the output of these gates. This leads to less spurious SUM and Carry signal. The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. It should be noted that the new SERF adder has no direct path to the ground.

The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re- application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.

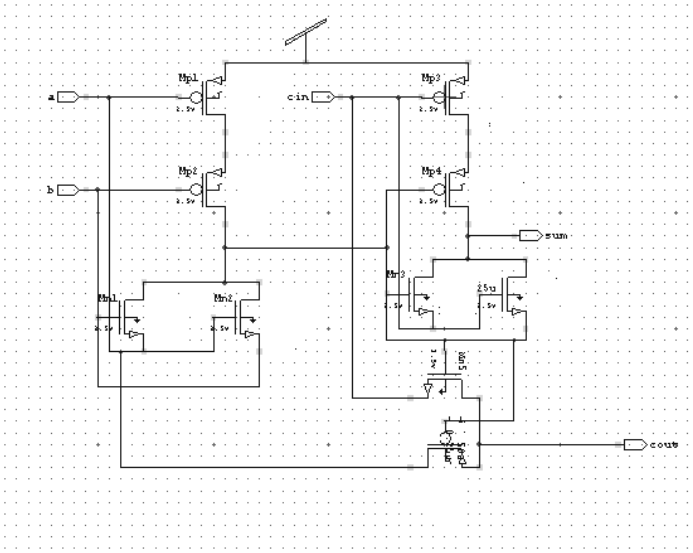

Figure 5: SERF Full Adder Circuit

Adder 9b

The Static Energy Recovery XNOR gate is cascaded with the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits

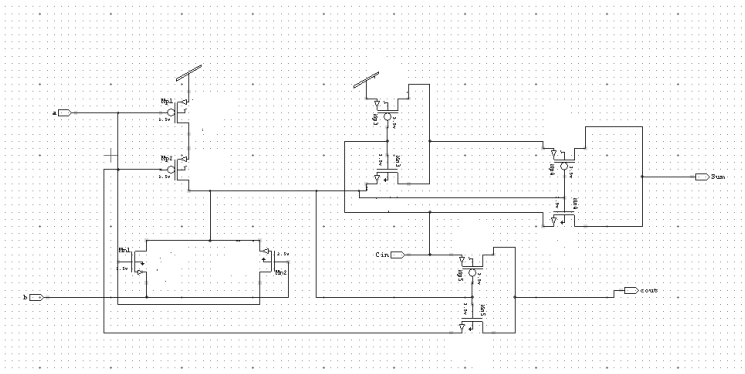

Figure 6: Adder 9b Circuit

GDI Based XOR and XNOR 10T Full Adders

The main difference between the CMOS and GDI based design is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. This feature gives the GDI cell two extra input pins for use which makes the GDI design more flexible than CMOS design.

GDI cell consists of three inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both nMOS and PMOS are connected to N and P respectively. Table 1 shows different logic functions implemented by GDI logic [15] based on different input values. So by using GDI technique we can implement various logic functions with less power and high speed as compared to conventional CMOS design

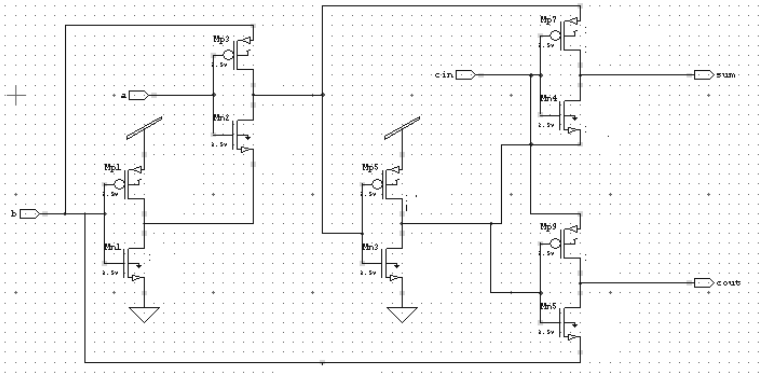

Figure 7: GDI based XOR 10T Full Adder Circuit

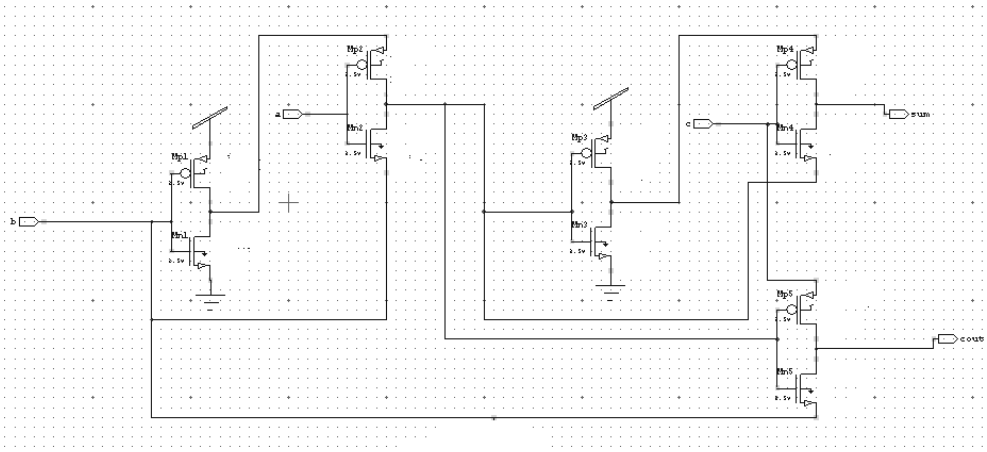

Figure 8: GDI Based XNOR 10T Full Adder Circuit

In Figure 7 and Figure 8. A, B and Cin are taken as input and output of the circuit is drawn from the Sum and Cout. Mp1, Mp2, Mp3, Mp4, and Mp5 are the PMOS transistors whereas Mn1, Mn2, Mn3, Mn4, and Mn5 are the NMOS transistors.

The implementation of XOR and XNOR gate are using GDI technique. It is the main building block of full adder circuit. So if optimize the XOR and XNOR gate then it can improve the overall performance of the 1 bit full adder circuit.

G. Proposed SRLGDI based XNOR Full Adder

Addition is an indispensable operation for any high speed digital system and control system. The primary issues in the design of adder cell are area, delay and power consumption. A, B and Cin are taken as input and output of the circuit sum and carry .The sum logic is evaluated by XNOR gate and carry logic is realized using MUX.

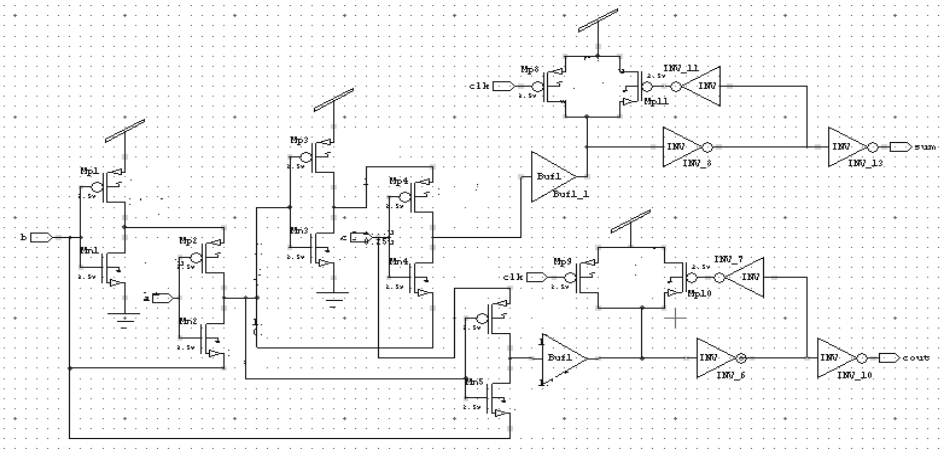

Figure 9: SRLGDI Based XNOR Full Adder Circuit

The self resetting logic circuit operation is defined in two phases as precharged and evaluation, such as PMOS precharged and reset transistor. During the precharged phase CLK=0 the GDI block is open, the transistor Mp8 is ON. The direct impedance path exists between node and VDD thereby charging the capacitance to VDD. For the evaluation phase CLK= 1 the GDI logic is closed, the transistor Mp8 is OFF and the output capacitance is charged. This voltage is fed through the delay path and produces Mp11 is active after the specified delay path. The Mp11 transistor recharges the node capacitor back up to a voltage of node is VDD.

Comparative Charts

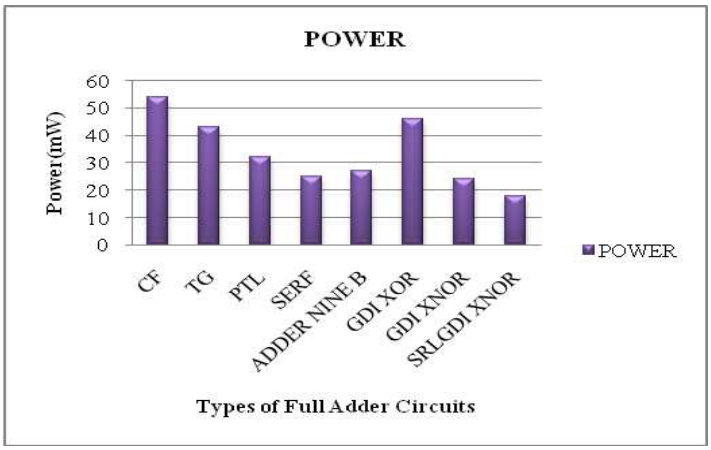

Figure 10: Power of the Different Types of Full Adder Circuits

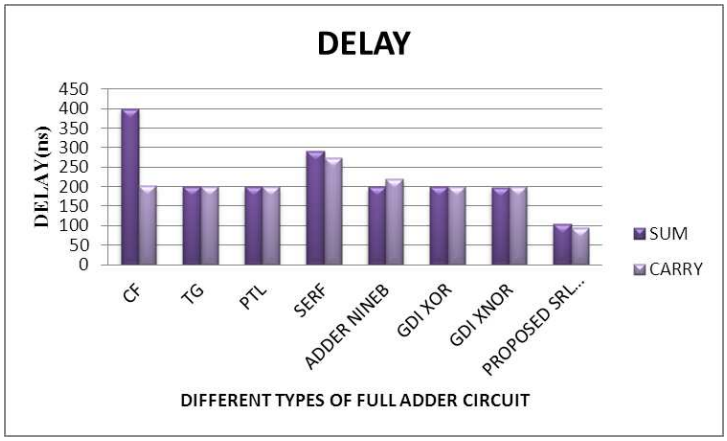

Figure 11: Delay of the Different Types of Full Adder Circuits

SIMULATION RESULT

The most conventional 28 transistors full adder, 20T, 14T, 10T and the other conventional full adder cells (Static Energy Adder (SERF), Adder9B, GDI based Full adder) are all simulated using S-Edit, T-Spice and W-Edit in 250nm CMOS technology.

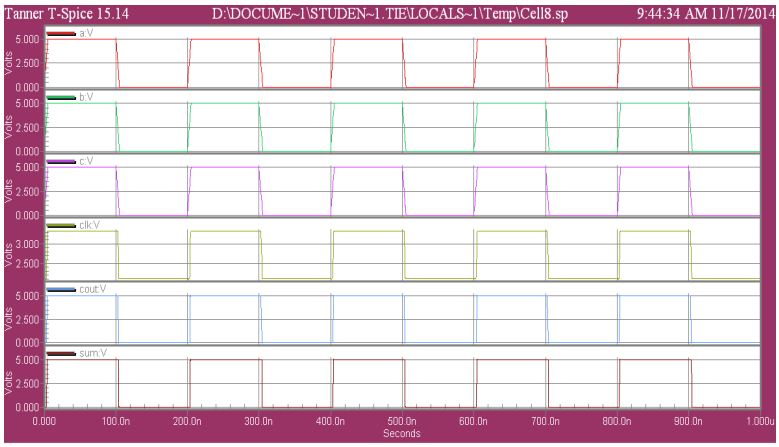

Figure 12: Simulation Waveform

Table 2: Power Consumption

Different Types of Full Adders	Power Consumption (mW)
Conventional 28T CMOS Full Adder Circuit	54
Transmission Gate Full Adder	43
Pass Transistor Full Adder	32
Static Energy Recovery Full Adder Circuit	25
Adder 9B	27
GDI Based 10T XOR Full Adder	46
GDI Based 10T XNOR Full Adder	24
Proposed SRLGDI Based XNOR Full Adder	18

Table 3: Delay

Different Types of Full Adders	Delay (ns)	
	Sum	Carry
Conventional 28T CMOS Full Adder Circuit	399.573	201.443
Transmission Gate Full Adder	200.31	200.01
Pass Transistor Full Adder	199.00	199.00
Static Energy Recovery Full Adder Circuit	290.895	274.28
Adder 9B	199.73	220.52
GDI Based 10T XOR Full Adder	199.79	199.995
GDI Based 10T XNOR Full Adder	198.77	199.56
Proposed SRLGDI Based XNOR Full Adder	103.681	94.342

CONCLUTIONS AND FUTURE SCOPE

From the analysis of the above various type of Full Adder Circuits. It can be concluded that the average power and delay are low in SRLGDI type Full adder.

In future, these presented results will encourage the researchers for further research activities on GDI techniques. To reduce power of a SRLGDI based adder cell some more circuit level power management techniques should be used so that it can be useful for low power applications. Implementation of different kinds of mixed and digital circuits have to be carried out in order to determine the fields of circuitry, where SRLGDI is very much superior over other design styles.

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